(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: 0 459 493 A2

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 91108886.2

(51) Int. Cl.5: H01L 23/495, H01L 23/498

(22) Date of filing: 31.05.91

(30) Priority: 01.06.90 JP 141684/90

(43) Date of publication of application:
04.12.91 Bulletin 91/49

(84) Designated Contracting States:
DE FR GB

(71) Applicant: Kabushiki Kaisha Toshiba
72, Horikawa-cho Saiwai-ku
Kawasaki-shi(JP)

(72) Inventor: Fujitsu, Takao, c/o Intellectual Property Div.
K.K.TOSHIBA, 1-1 Shibaura 1-chome,
Minato-ku
Tokyo 105(JP)

(74) Representative: Lehn, Werner, Dipl.-Ing. et al
Hoffmann, Eitle & Partner Patentanwälte
Arabellastrasse 4
W-8000 München 81(DE)

(54) A semiconductor device using a lead frame and its manufacturing method.

(57) A plurality of electrode pads (14) are formed on a main surface of a semiconductor chip (11). The electrode pads (14) on the semiconductor chip (11) are electrically connected to the top end of an inner lead (19) through a metal plating layer (20).

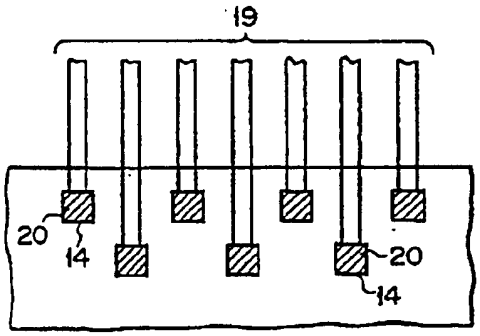


FIG. 7

EP 0 459 493 A2

an electrolytic plating solution and forming a metal plating layer where the lead frame is electrically connected to the electrode on the semiconductor chip.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a cross sectional view showing the structure of a part of a device of a first embodiment of the present invention;

Fig. 2 is a cross sectional view showing a general structure of the device of the first embodiment of the present invention;

Fig. 3 is a cross sectional view showing a specific structure of an electrode pad of the device of the first embodiment of the present invention;

Fig. 4 is a plane view showing a state of the connection between a plurality of electrode pads of the device of the first embodiment and a plurality of inner leads;

Figs. 5 and 6 are plane views of a TAP tape, which is used in the device of the first embodiment of the present invention, respectively;

Figs. 7 and 8 are plane views of modifications of the device of the first embodiment of the present invention, respectively;

Fig. 9 is a cross sectional view showing a device of a second embodiment of the present invention;

Fig. 10 is a cross sectional view showing a device of a third embodiment of the present invention; and

Fig. 11 is a cross sectional view showing a device of a fourth embodiment of the present invention.

The embodiments of the present invention will be explained with reference to the drawings.

Fig. 1 shows the structure of a part of a semiconductor device of a first embodiment of the present invention wherein the present invention is used in the connection between a plurality of electrode pads on a semiconductor chip and a plurality of inner leads, and Fig. 2 is the general structure thereof.

In the drawings, reference numeral 11 is a semiconductor chip wherein an active element such as a transistor and a passive element such as a resistor and a capacity. Around the main surface of the semiconductor chip 11, there are formed a plurality of electrode pads 14, which is formed of a first metal layer 12 whose lower layer is formed of aluminum (Al) and a second metal layer 13 whose upper layer includes at least one nickel layer. These electrode pads 14 are arranged in line with a predetermined distance. The portions of the semiconductor chip 11 other than the electrode pad formation position are covered with an insulating surface protection film 15 such as a silicon oxidation film. The semiconductor chip 11 is adhered to a predetermined portion of a TAB tape 17 by an epoxy adhesive 16.

As shown in Fig. 1, the TAB tape 17 is made of epoxy or polyimide resin. Metal foil such as copper (Cu) foil having a thickness of about 35 μm is laminated on an organic film material 18 having a thickness of about 75 μm. Thereafter, there is formed a wiring pattern comprising a plurality of inner leads 19 to be connected to the plurality of electrode pads 14 by a selection etching technique and outer leads electrically connected to these inner leads (not shown). The wiring pattern forming surface is adhered to the semiconductor chip 11 by the adhesive 16.

When the semiconductor chip 11 is adhered to the TAB tape 17, the positioning is performed in a state that each electrode pad 14 is positioned close to the portion where each end surface of the end portions of the plurality of inner leads 19 is exposed. Then, each electrode pad 14 on the semiconductor chip 11 and each end portion of the inner lead 19 are electrically connected through a metal plating layer 20 formed of nickel (Ni).

Fig. 3 shows the specific structure of each electrode pad 14. In this embodiment, the second metal layer 13 formed on the first metal layer 12 made of aluminum (Al) comprises at least two metal layers. More specifically, the lower layer contacting the first metal layer made of aluminum is formed of a titan (Ti) layer 31 having a thickness of 1000 Å, and the upper layer is formed of the nickel (Ni) layer 32 having a thickness of 3000 Å. The nickel layer 32, which is the upper layer of the second metal layer 13 is formed to allow the metal plating layer 20 made of nickel to be formed on the electrode pad 14. Also, the titan layer 31, which is the lower layer of the second metal layer 13, has a function as barrier metal.

Fig. 4 shows a state of the connection between the plurality of electrode pads 14 and the plurality of inner leads 19 formed on the TAB tape 17. In the drawing, a region in which slant lines are added shows the metal plating layer 20.

In the above embodiment, each electrode pad 14 on the semiconductor chip 11 and each inner lead 19 are connected by the metal plating layer 20. Due to this, bonding capillary and TAB tool, which are used to the wire bonding and TAB connection are not required. Thereby, the distance between electrode pads 14 can be reduced to 100 μm or less, for example, about 50 μm.

Moreover, if each electrode pad 14 and each inner lead 19 are electrically connected, no physical pressure is applied to the semiconductor chip 11, so that resistance due to pressure damage is not allowed. Then, since a large number of portions

can be connected at the same time under the same condition, reliance of connection can be improved. Moreover, since there is no need of heating when the connection is performed, it is possible to prevent reliance from being lowered by thermal stress, which is caused by a mismatch of the coefficient of thermal expansion of each semiconductor layer in the semiconductor chip.

A method of forming the above metal plating layer where the electrode pads and the inner leads are electrically connected will be explained.

In TAB tape, as shown in Fig. 5, metal foil such copper foil is laminated on the organic film material 18 in advance. Thereafter, in every semiconductor device, there are formed a plurality of lead electrodes 41 comprising the inner leads and the outer leads connected to the inner leads by the selection etching technique. At the same time when the selection etching is performed, common electrodes 42, which are electrically connected to the lead electrodes 41, are formed around each semiconductor device in a state that all common electrodes 42 are connected. Additionally, in Fig. 5, reference numeral 43 is an opening formed in the organic film material 18.

Fig. 6 shows an enlarged one semiconductor device in the TAB tape of Fig. 5 In the drawing, the semiconductor chip is adhered to TAB tape In a state that the semiconductor chip is positioned in the area shown by a one dotted chine line. In this case, the semiconductor chip is adhered to TAB tape so that the pad of each electrode on the semiconductor chip is positioned close to the portion where each end of the end portion of the plurality of leads is exposed.

Thereafter, TAB tape is immersed in nickel plating bath together with a plating electrode. The nickel plating bath is generally called a watt bath, and nickel sulfate, nickel chloride, and adhesive are used. After TAB tape and the plating electrode are immersed in the watt bath, a predetermined direct voltage is applied between the common electrode 42 and the plating electrode in order that the common electrode 42 serves as a positive side and the plating electrode serves as a negative side, and electrolytic plating is performed for a predetermined period of time. For example, a direct voltage to be applied was set to 2V, a current to be supplied between the positive and negative sides was set to 60mA, and plating time was set to 10 minutes. As a result, a nickel plating layer having a thickness of 10 μm was obtained as metal plating layer 20. The metal plating layer grows from each end surface of the top end portion of the inner lead immediately after plating starts. Then, if the growth advances and the plating layer contacts the electrode pad on the semiconductor chip, the metal layer also grows in the lectrode pad, and both the common electrode 42 and the plating electrode are finally electrically connected by the plating layer. After the end of plating, the plating layer is washed with pure water, and contaminant, which was adhered to the surface when plating, is removed. Additionally, in the surface of each lead electrode 41, which comprises the inner and outer leads, the most of the surface other than the top end portion of the inner lead is coated with an epoxy insulating film, which is called green coat. Thereby, it is possible to form the plating layer in only the necessary portion. Due to this, plating time can be shortened.

Various modifications of the first embodiment will be explained.

The above embodiment explained that the electrode pads were arranged in line with a predetermined distance. In the modified device of Fig. 7, the electrode pads 14 are arranged on the semiconductor chip in a zig-zag manner. The same reference numerals as Fig. 4 are added in the portions corresponding to the portions of Fig. 4, and the explanation thereof is omitted.

Fig. 8 shows a modification of the device using a semiconductor which is the so-called free access pad layout system wherein the electrode pads are arranged on the entire surface of the semiconductor chip at random.

As mentioned above, the present invention can be used in any type of chip regardless of the arrangement of the electrode pads on the chip.

Next, other embodiments of the present invention will be explained.

Fig. 9 shows the structure of the semiconductor device relating to a second embodiment of the present invention wherein the present invention is used in the connection between the outer leads of the lead frame and the wiring pattern on the print circuit board. In the drawing, reference numeral 11 is a semiconductor chip, and reference numeral 17 is a TAB tape. In this embodiment, the top end portion of the inner lead of the TAB tap and electrode pad (not shown) on the semiconductor chip 11 are electrically connected by a metal plating layer 20 similar to the first embodiment. According to the second embodiment, a wiring pattern 52, which is formed on a print circuit board 51, and the outer lead of the TAB tape are also electrically connected by the metal plating layer 20.

Fig. 10 shows the structure of the semiconductor device relating to a third embodiment of the present invention wherein the present invention is used in the connecti n between the outer leads of the lead frame and th wiring pattern on the print circuit board. According to th third mbodiment, the lead frame is formed by punching a metal thin film, which is formed of alloy such as 4-2 alloy and copper by a press process. An inner lead 53 of the

lead frame and an electrode pad 14 on a semiconductor chip are electrically connected by use of both a conductive adhesive 54 and a metal plating layer 55. In the case of the first embodiment using the TAB tape, the metal plating layer can be formed in a manner that the semiconductor chip is adhered to the TAB tape by the adhesive in advance. In the case of using the lead frame formed by punching the metal thin film, the adhesive 54 is formed on each electrode pad 14 in advance by a screen printing method and the electrode pad 14 and the lead frame 53 are adhered by the adhesive 54. Thereafter, the plating layer 55 is formed by the same method as mentioned above, and both the electrode pad and the lead frame can be electrically connected.

As mentioned above, the present invention can be used in not only the connection between the inner lead of the lead frame and the electrode pad on the semiconductor chip but also the connection between the outer lead and the wiring pattern on the print circuit board, and the same effect can be obtained. Moreover, the present invention can be used in the electrical connection between a liquid crystal display and TAB tape.

The present invention is not limited to the above-mentioned embodiments. It is needless to say that the present invention can be variously modified. For example, in the above embodiments explained the case wherein the metal plating layer was the nickel plating layer. According to the present invention, Au plating layer and copper plating layer can be used in addition to the above case.

The above first embodiment explained the case wherein the most of the surface other than the top end portion of the inner lead was coated with the insulating film in advance. However, in the portion other than the top end portion of the inner lead, the thickness of which the plating layer can grow on the above portion is about only 1/10 times that of the top end portion when the electrolytic plating is performed, the adherence of the insulating film can be omitted.

Moreover, the method of the above embodiment explained the case that the plating layer was formed by the electrolytic plating method. However, the plating layer can be formed by an electrolessly plating method.

Fig. 11 is a cross sectional view showing a device of a fourth embodiment of the present invention. The above embodiments explained the case in which two wirings are connected to each other by the plating metal. However, this plating metal can be used as a sealing for the semiconductor device. The device of the fourth embodiment shows that the plating lay r is used as a sealing for a cap of a PGA (Pin Grid Array) typed semiconductor device. In Fig. 11, a package 61 is formed by layering tow ceramic plates 62 and 63. On one ceramic plate 62, a concave portion 64 is formed, and a semiconductor chip 65 is contained in the concave portion 64. Also, a plurality of wirings 66, 66, ... are formed on the surface of one ceramic plate 62. Moreover, there are formed a plurality of pads (not shown) on the surface of the semiconductor chip 65. Then, the plurality of pads on the semiconductor chip 65 and the plurality of wirings 66, 66 ... are connected by metal wires 67, 67 ..., respectively.

On the other ceramic plate 63, there is formed an opening 68 having an area larger than the concave portion 64 at the position corresponding to the concave portion 64 of one ceramic plate 62. The opening 68 forms the concave portion 64 and the containing section of the semiconductor chip 68. Then, on the surface of the ceramic plate 63 around the opening 68, there is formed, for example, an Fe - Ni metal layer 69. Moreover, the opening 68 of the ceramic plate 63 is covered with a cap 70. The metal layer 69 and the cap 70 are adhered to each other by a metal plating layer 71 formed of nickel. The metal plating layer 71 is also formed between the cap 70 and the metal layer 69 and on the entire exposed surface.

As mentioned above, the metal plating layer can be used as a sealing for the cap.

Claims

1. A semiconductor device characterized by comprising:

   a lead frame (19; 53) formed of a conductive material;

   a semiconductor chip (11) having a plurality of electrodes (14) on its surface; and

   a connect section (20) where said lead frame is electrically connected to said plurality of electrodes on the semiconductor chip by a metal plating.

2. The semiconductor device according to claim 1, characterized in that said lead frame (19) is a TAB type in which a wiring pattern is formed on an insulating film (18).

3. The semiconductor device according to claim 1, characterized in that said lead frame (53) is formed by punching a metal film.

4. The semiconductor device according to claim 1, characterized in that said plurality of electrodes (14) formed on th surface of said semiconductor chip comprise an aluminum layer (12), a titan layer (31) formed on said aluminum layer (12), one layer (32) of a metal

layer formed on said titan layer, a nickel layer, or a copper layer.

5. The semiconductor device according to claim 1, characterized in that said plurality of electrodes are arranged on said semiconductor chip in a zig-zag manner.

6. The semiconductor device according to claim 1, characterized in that said plurality of electrodes are arranged on said semiconductor chip at random.

7. A semiconductor device characterized by comprising:

an insulating film (18);

a wiring pattern (19) formed on said insulating film;

a semiconductor chip (11) having a plurality of electrodes (14) on its surface; and

a connect section (20) where the end surface of said wiring pattern is electrically connected to said plurality of electrodes on said semiconductor chip by a metal plating.

8. The semiconductor device according to claim 7, characterized in that said plurality of electrodes (14) formed on the surface of said semiconductor chip comprise an aluminum layer (12), a titan layer (31) formed on said aluminum layer (12), one layer (32) of a metal layer formed on said titan layer, a nickel layer, or a copper layer.

9. The semiconductor device according to claim 8, characterized in that said plurality of electrodes are arranged on said semiconductor chip in a zig-zag manner.

10. The semiconductor device according to claim 8, characterized in that said plurality of electrodes are arranged on said semiconductor chip at random.

11. A semiconductor device characterized by comprising:

a semiconductor chip (11);

a plurality of leads (17) electrically connected to said semiconductor chip;

a wiring board (51) having a wiring pattern (52) on its surface; and

a plurality of connect sections (20) where said plurality of leads are lectrically connected to said wiring pattern on said wiring board by a metal plating.

12. A semiconductor device characterized by comprising:

a lead frame (53) formed of a conductive material;

a semiconductor chip (11) having an electrode (14) on its surface;

a first connect section (54) where said lead frame is electrically connected to an electrode on said semiconductor chip by a conductive adhesive; and

a second connect section (55) where said lead frame is electrically connected to said electrode on said semiconductor chip by a metal plating to cover the surroundings of said first connect section.

13. A method of manufacturing a semiconductor device comprising the steps of:

moving a lead frame (19) formed of a conductive material and an electrode (14) formed on a surface of a semiconductor chip (11) to be close to each other, and adhering said semiconductor chip to said lead frame; and

immersing said lead frame and said semiconductor chip in an electrolytic plating solution, and forming a metal plating layer where said lead frame is electrically connected to said electrode on said semiconductor chip.

14. The method according to claim 13, characterized in that said lead frame (19) is formed of a plurality of lead electrodes (41), said plurality of lead electrodes (41) are electrically connected by a common electrode (42), and an electric potential is supplied to said common electrode (42) when said metal plating layer is formed.

15. A semiconductor device characterized by comprising:

a package (61) formed of an insulating material and having a containing portion (64, 68) of a semiconductor chip;

a conductive layer (69) formed around said containing portion of said case;

a cap (70) formed on said containing portion of said package; and

a metal plating layer (71) connecting said cap (70) to said conductive layer (69).

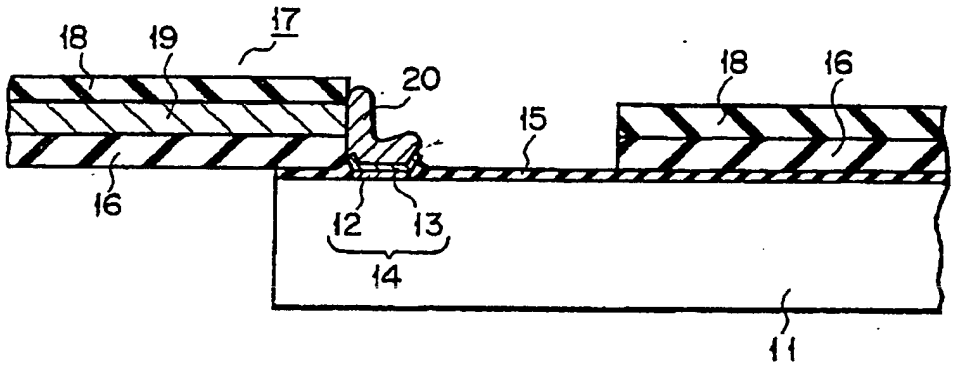


FIG. 1

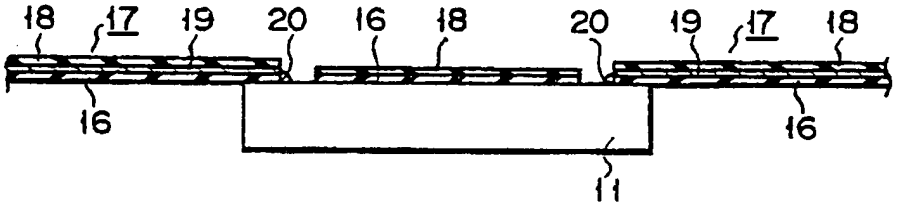


FIG. 2

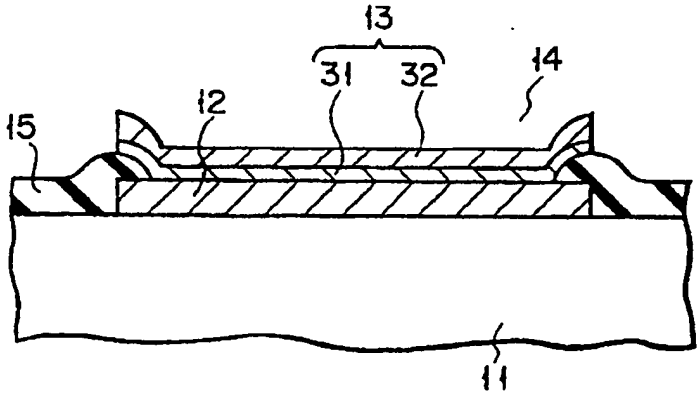


FIG. 3

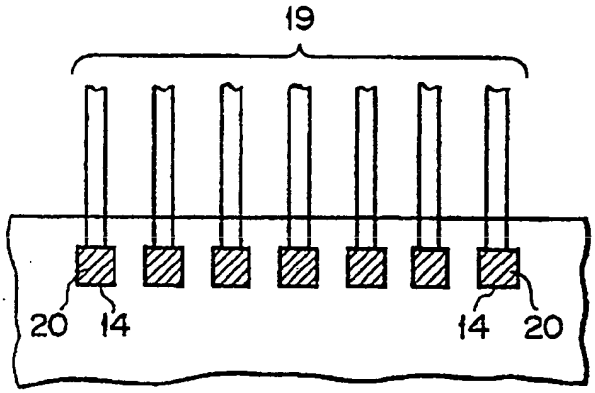


FIG. 4

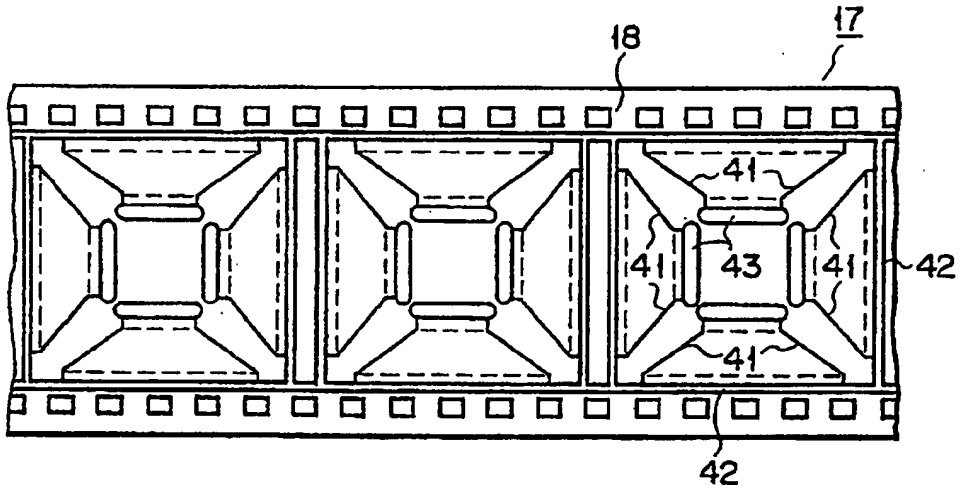


FIG. 5

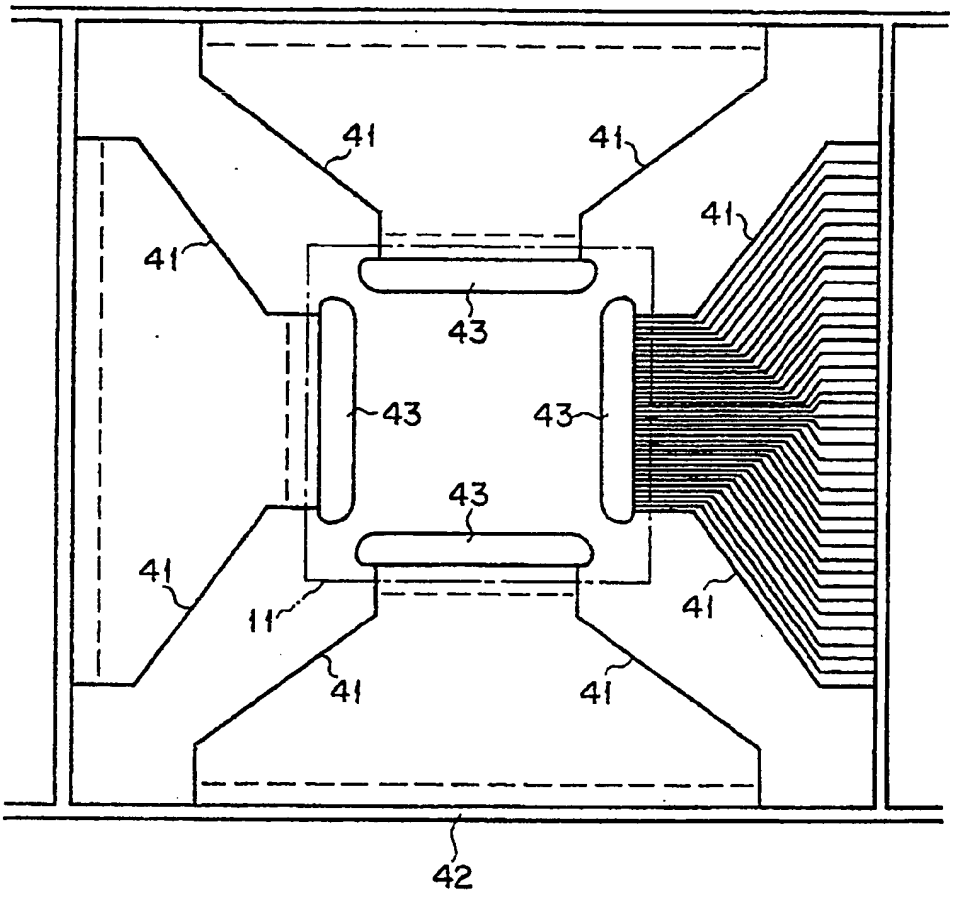


FIG. 6

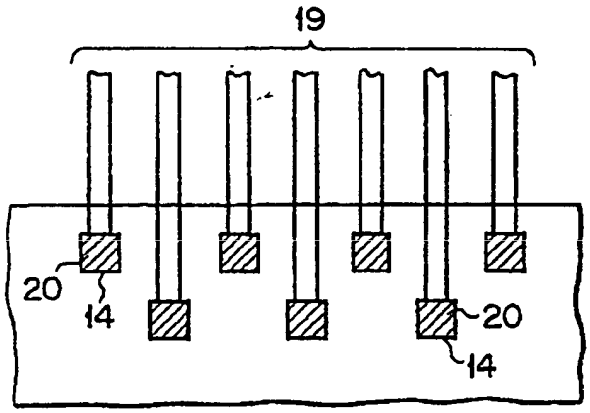


FIG. 7

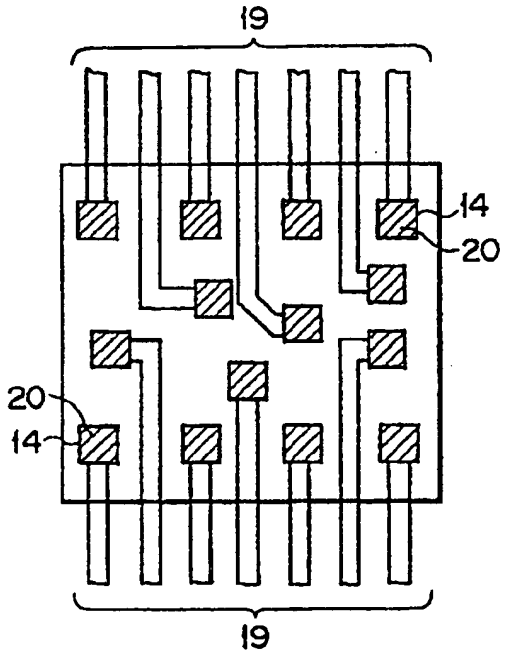


FIG. 8

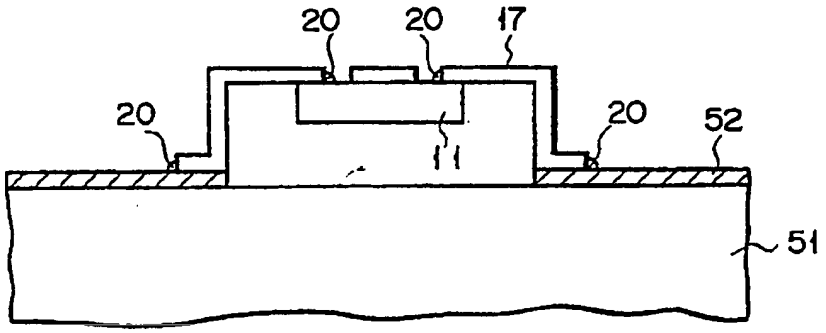


FIG. 9

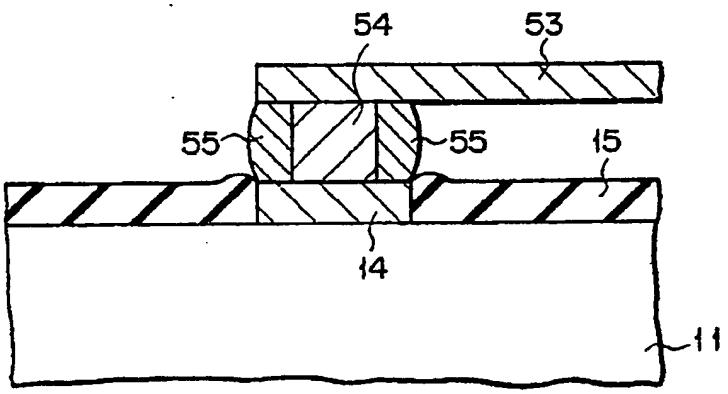


FIG. 10

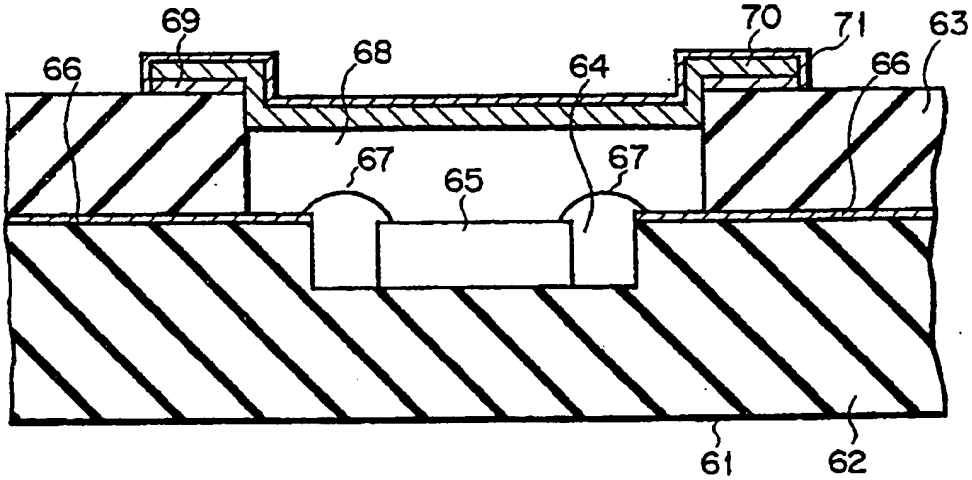


FIG. 11

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 393 997 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 90304121.8

(51) Int. Cl.5: H01L 23/495

(22) Date of filing: 18.04.90

(30) Priority: 20.04.89 US 341638

(43) Date of publication of application:
24.10.90 Bulletin 90/43

(84) Designated Contracting States:
DE FR GB

(71) Applicant: HONEYWELL INC.
Honeywell Plaza
Minneapolis Minnesota 55408(US)

(72) Inventor: Dunaway, Thomas J.
2512 Highway 100 South
St. Louis Park, Minnesota 55416(US)
Inventor: Poplett, James M.
15752 27th Avenue North
Plymoth, Minnesota 55447(US)
Inventor: Spielberger, Richard K.
17814 83rd Avenue North
Maple Grove, Minnesota 55369(US)

(74) Representative: Fox-Male, Nicholas Vincent Humbert
Honeywell Control Systems Limited Charles Square
Bracknell Berkshire RG12 1EB(GB)

(54) Package to board variable pitch tab.

(57) A variable pitch tab leadframe assembly (103) has a plurality of patterned conductive elements (107) for transmitting input and output signals to bonding locations on an electronic device. The leadframe assembly comprises conductive elements with a variable pitch to accommodate a plurality of standard pitch bond site printed circuit board footprints.

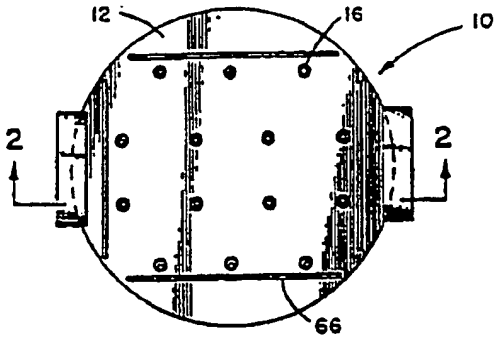


FIG. 1

EP 0 393 997 A2

PACKAGE TO BOARD VARIABLE PITCH TAB

Field of the Invention

The present invention relates to the field of electronic component manufacturing and packaging.

Background of the Invention

A problem in the prior art of electronic component packaging includes inefficient steps in the production of leadframes for bonding with variably sized and pitched component packages. The substantial inefficiencies inherent in requiring different leadframes to be manufactured for connecting different packages to printed circuit boards is both costly and wasteful. However, by providing a universal tab leadframe which may be utilized, by only slight modification, with variably pitched packages, then cost and material savings combine to greatly improve the manufacturing and packaging processes. The present package to board variable pitch tab leadframe invention overcomes the problems identified above.

Summary of the Invention

The present invention is a variable pitch tab leadframe assembly. The leadframe assembly comprises a plurality of patterned conductive elements for transmitting input and output signals to bonding locations on an electronic device. The leadframe assembly comprises conductive elements with a variable pitch to accommodate a plurality of standard pitch bond site printed circuit board footprints.

Brief Description of the Drawings

Figure 1 is a top plan view of a shadow mask and die assembly showing shadow mask vias.

Figure 2 is a side elevation cross section view taken generally along line 2-2 of Figure 1 showing a shadow mask removably attached to a die representing a wafer or chip.

Figure 3 is an enlarged cross sectional elevation view of a portion of the di shown in Figure 2 illustrating deposited solderable material on a portion of the die after the mask is removed from the die.

Figures 4a and 4b are cross section elevation views of a prior art leadframe/gold bump bonding process showing both incomplete leadframe-to-gold bump bonding and a fractured die.

Figures 5a and 5b are cross section elevation views of a leadframe with organic standoff means arranged for bonding with solder bumps.

Figure 6 is a side elevation view depicting a schematic prior art tin coated copper leadframe being positioned for bonding to a gold metalization bump.

Figure 7 is a side elevation view depicting a schematic copper leadframe shown in position for bonding to a tin cap solid base metalization bump.

Figure 8 is a cross section elevation view of a prior art gold bump manufactured by a spin-on resist process.

Figure 9 is a cross section elevation view of a spun-on resist solid base bump with a tin cap.

Figure 10 is a cross section elevation view of a prior art vertical wall gold bump manufactured by a dry film resist process.

Figure 11 is a cross section elevation view of a vertical wall dry film resist solid base bump with a tin cap.

Figure 12 is a top fragmentary view of a variable pitch tab leadframe.

Figure 13 is a top plan view of a representative tape leadframe illustrating four sections generally analogous to that shown in Figure 6 to form a complete variable pitch tab leadframe about a central package area.

Figure 14 is a top plan schematic view of the second end portions of adjacent conductive elements of a variable pitch tab leadframe having a first pitch at bond pads of a next level of packaging.

Figure 15 is a top plan schematic view of the second end portions of adjacent conductive elements of a variable pitch tab leadframe having a second pitch at bond pads of a next level of packaging.

Figure 16 is a top plan schematic view of the second end portions of adjacent conductive elements of a variable pitch tab leadframe having a third pitch at bond pads of a next level of packaging.

Detailed Description of the Preferred Embodiments

Detailed preferred embodiments of the present invention are disclosed. It is to be understood.

however, that the disclosed embodiments are merely exemplary of the invention, which may be embodied in various forms. Therefore, specific structural and functional details disclosed are not to be interpreted as limiting, but rather as a representative basis for teaching one skilled in the art to variously employ the present invention in virtually any appropriately detailed system or structure. It will be understood that in some circumstances relevant material thicknesses and relative component sizes may be shown exaggerated to facilitate an understanding of the invention.

Inventions described in the present application relate to improvements in manufacturing, bonding, and packaging of electronic components to achieve improved reliability, improved yield, and greater material and manufacturing efficiencies. The improvements comprise unique features including etched shadow mask construction, conductive metalized bump composition, and preferred structure of tape leadframes.

Referring to Figure 1, an exemplary mask 10 is illustrated. It is appreciated that masks, also known as shadow masks or vapor deposition masks, are variously constructed and shaped; however, the basic function of masks is to provide vapor deposition patterns for conductive material to be evaporated onto a die thereunder. Accordingly, mask 10 comprises a mask top surface 12 which defines apertures or vias 16. Mask 10 is removably mounted on a surface of a die and positioned in a chamber in which evaporation and deposition of solderable material will occur. During the evaporation and deposition process, the solderable material passes through vias 16 in mask 10 and is deposited in a pattern on the die. This provides a pattern of solderable material on the die for later reflowing, bonding, or other operations.

Frequently, prior art masks experience warping or other reshaping so that vaporized solderable material passes through the vias and is deposited on various portions of the die which were not directly beneath each via area. This results in unwanted electrical shorts being created on the die. Yet another problem exists with prior art masks wherein a substantial portion of the mask surface is in contact with the die when the mask is agitated or slightly moved. This often results in scratching of the die surfaces. These problems substantially reduce the yield of reliable die during the production process. Due to the expensive recovery required in repair f poorly manufactured or damaged dies, many such devices are discarded. It is appreciated, therefore, that the associated yield problem results in waste and inefficiency in the industry.

Figure 2 is a side elevation cross section view taken generally along lines 2-2 of Figure 1 showing mask 10 removably mounted onto die 24 by mounting means 20. Die 24 may comprise a semiconductor chip, or a wafer comprising numerous semiconductor chips. Die 24 may comprise various materials and layers, however, a representative material combination in the die upper passivation region 25 includes a passivation portion 25a, such as silicon nitride, or more generally an insulator material, and a metalized portion 25b, such as aluminum, or more generally a conductive metallization. As is well known in the field, metalized portions 25b comprise conductive interconnects and are, therefore, deposition sites for later depositing of the vaporized solderable material. More specifically, interface metalization 28, shown in Figure 3, is commonly deposited first onto metalized portion 25b, and then solderable bump material 30, also shown in Figure 3, is then vapor deposited through vias 16 onto interface metalization 28.

Figure 2 shows die 24 comprising top surface 34 and bottom surface 36. Figures 2 and 3 therefore illustrate die 24 having a plurality of deposit sites etched or otherwise positioned to provide solderable material in the form of bumps onto interface metalization 28, and extending generally from die top surface 34. In order to precisely position vaporized solderable material at these particular desired deposition sites, a mask of suitable rigidity and via pattern must be used. Such masks are frequently made of metallic materials, as preferably is mask 10, which is typically constructed of molybdenum; however, other materials may be utilized such as glass or plastic.

Mask 10 comprises mask top surface 12 which functions as an outer surface facing away from die 24 in operation, and which is located opposite mask bottom surface 13. As shown in Figure 2, vias 16 extend through mask 10 between top surface 12 and bottom surface 13 to permit vaporized bonding metals to pass through the mask and to deposit onto predetermined locations of die 24. As further shown in Figure 2, mask bottom surface 13 comprises a plurality of recessed regions 44. Regions 44 are constructed to minimize the area of mask 10 in contact with die 24 during the vapor deposition process. Moreover, the arrangement of recessed regions 44 in relation to bottom surface 13 surrounding vias 16 provides for substantially full mask thickness via regions having a width labelled R which provide damming action about the via to retain the vapor deposit within the predetermined deposit sites of die 24 defined by the via regions.

Another way of describing the relation between recessed regions 44 and vias 16 is to describe the recessed regions 44 as having a base surface 47 which ar constructed and arranged for placement at a distance D from die surface 34. Thus, mask 10 bottom surface 13 includes etched recessed re-

gions 44 which define a projection 49 located around each via 16. Projections 49 extend from the plane or planes 50 which includes base surfaces 47 of etched recessed regions 44 to minimize the contact area of mask 10, to only that area of bottom surface 13, in contact with die 24 during the entire process of vapor deposition.

By reducing the surface area of mask 10 actually in contact with die 24, the risk of the mask damaging the die is greatly reduced. Moreover, this mask construction allows the clamping or retaining force of mounting means 20 to be advantageously focused onto the areas defined by bottom surface 13 immediately surrounding vias 16. Thus, a secure fit of mask 10 results and unwanted deposition of solderable material beyond the area on the die defined by the diameters of each via 16, shown in Figure 2 as R', is prevented. Prior art shadow masks have failed to adequately contain solderable materials and have frequently resulted in undesired and uncontrolled seepage of such materials between predetermined deposition sites, resulting in electrical shorts and reduced capabilities of the devices involved.

It is to be understood that as the number of vias on mask 10 increases, an increasing area of mask bottom surface 13 is required to achieve the objectives stated above. Also, as the density of vias 16 increases, then undesired flexing or loss of rigidity of mask 10 may occur. Therefore, reinforcing ridges 66, shown in Figures 1 and 2, may be utilized for stiffening mask 10. Reinforcing ridges 66 may be arranged in various orientations and shapes to achieve the advantages within the scope of this invention. Indeed, reinforcing ridges 66 need not be limited to protrusions from top surface 12 but instead may comprise material which is hardened in relation to the mask material comprising the remainder of mask 10.

In a preferred embodiment, mask 10 comprises a molybdenum mask having a full thickness of 4 mils. Preferred mask 10 may be used with a die having passivation and metalization combined thickness of approximately 20 mils. Moreover, such a combination would provide means for depositing about a .5 micron thin film interface metalization 28, and a subsequent 100 micron thickness solderable material 30, as shown generally and not to scale in Figure 3. It is appreciated that sizes and shapes shown herein may vary considerably with each production requirement. The substantial reduction of contact surface ar a between mask 10 and die 24 is most relevant, as is the manner in which mask 10 prevents unwanted deposition of conductive metalization nto areas of die 24 beyond the via areas labelled by diameter R'.

A method of manufacturing a damage reducing tched shadow mask 10 for providing vapor deposition patterns of bonding metals onto a surface of die 24 is also provided. This method preferably comprises the steps of providing a nonwettable shadow mask 10 having top surface 12 and bottom surface 13; creating vias 16 extending through mask 10; and etching portions of mask 10 bottom surface 13 to provide recessed regions 44 and substantially full thickness regions (having height labelled E and width comprising the thickness of R-R' as shown in Figure 2), the recessed regions 44 providing for a reduced surface area in contact with die 24 during a vapor deposition process. The etching step may further comprise providing projections 49 or ridges extending annularly from vias 16 at bottom surface 13 of mask 10. Mask 10 permits manufacture and deposition through evaporation of a plurality of bumps comprising solderable conductive bump material 30, Figure 3, and which is shown in shadow 31 in a reflowed configuration.

Within the field of electronic component manufacturing and packaging, serious problems exist due to inadequate uniformity of conductive bump height, unacceptable organic matter within packages, fatigue-prone bonds, and temperature sensitive components. An example of non-uniform conductive bump heights is shown in Figure 4a in which prior art gold bumps 61a, 61b, 61c, and 61d are arranged on die 62. As illustrated, bumps 61a, 61b, 61c, and 61d have different heights representative of the non-uniformity of bump heights often present in such structures. In a typical prior art process, a representative leadframe assembly is positioned over die 62 and the bumps, with the leadframe assembly comprising conductive metal leads 63.

Figure 4b illustrates the structures of Figure 4a after a planar bonding force has been applied to leads 63 by bonding tip means 66. As is shown in the figure, the bonding force has caused die 62 to fracture below gold bump 61b due to the high bump height of that bump. As is also shown, leads 63 have contacted and bonded with correspondingly located bumps 61b and 61d. However, gold bump 61c has not bonded with its lead due to the short bump height of bump 61c. This results in non-conductivity and improper performance of a device using die 62 and relying on a bond between bump 61c and its lead.

Figure 5a and 5b are cross section elevation views of a leadframe with organic standoff means arranged for bonding with solder bumps. Height standoff means 64 is commonly provided to prevent overcompression of leads 63 into the conductive bonding material of relatively soft bumps such as solder bumps 61e which do not maintain a uniform standoff height when bonding tip means 66 is brought into contact with leads 63 to form a

connection between leads 63 and die 62 via the solder bump 61e. Height standoff means 64, or dielectric means, is frequently constructed of organic material which is subject to moisture collection and long term deterioration.

The present tin cap on solid base bump invention solves the problems illustrated in Figures 4b and 5b. With the present tin cap on solid base bump invention, cracking of die 62 under prior art gold bumps such as 61b is substantially reduced when such prior art gold bumps are replaced by the present tin cap on solid base bump invention. Further, open connections such as shown above prior art gold bump 61c in Figure 4b are substantially reduced when such prior art gold bumps are replaced by the present tin cap on solid base bump invention. In addition, when the present tin cap on solid base bump invention is used to replace prior art solder bumps 61e, height standoff means 64 comprising organic material can be eliminated, thus creating the option of a package free of organic material, consistent with requirements such as those of U.S. Department of Defense Military Standard 38510.

It is to be understood that within the field of electronic component manufacturing and bonding another problem exists with respect to inadequate means for strong and efficient bonding of leads to various devices. For example, the bonding forces and temperatures needed for bonding prior art leads often caused cracking of integrated circuit devices and open bonds. These phenomena led to plating of leads, commonly copper leads, with tin in order to lower the force and temperature requirements for bonding. However, that solution led to yet another problem known as whiskering, which occurred principally during the tin plating process. This problem relates particularly to copper leads 76 such as depicted in Figure 6 that are plated or coated with a solderable material 78 such as tin. Plated lead 76 is shown prior to bonding to a conductive metalized bump 80 located on a semiconductor device 82. This new problem was addressed in the art either by providing additional processes to achieve tin stress relief or by plating the copper or other metal leadframes with gold or other metals. Those solutions, however, are relatively very time consuming and expensive, and are therefore less preferable to the low cost solution of the present tin cap on solid base, such as gold, bump invention.

As illustrated in Figure 7, conductive lead 84, such as a portion of a conductive metalized leadframe, is provided. A schematic conductive metalized bump 98 is also shown positioned on a die 90. Bump 98 preferably comprises a bump lower portion 92 comprising a gold base material of substantially 100% by weight gold to provide a substantially fixed standoff height during the bonding process. Bump 98 preferably also comprises a bump upper portion 94 comprising an effective amount of tin deposited on a top surface 97 of the gold base material comprising the bump lower portion 92. Preferred tin cap on gold base bump 98 provides improved means for interconnecting electronic components and comprises improved fatigue and expansion coefficient properties over solder bumps on dies. This gold-tin combination bond provides a high strength reflowable alloy.

As an alternative to lower portion 92 comprising substantially 100% by weight of gold, a suitable base material may be comprised of at least one metal selected from a group consisting of chrome, nickel, titanium-tungsten, cobalt, and copper. Of particular relevance, however, is the manner in which the bump lower portion 92 provides effective standoff height during the bonding process and the manner in which the tin cap marerial permits lead travel well into the bump structures during the bonding process so that the bump height uniformity tolerances may be less severe. It is to be understood, however, that a tin cap on a solid base bump may be employed without using only a gold base. For example, as indicated above, a solid base of nickel or other suitable conductive material is within the scope of this invention.

Further, by use of preferred bump 98, the previously identified problems of the prior art are solved using a relatively inexpensive combination and arrangement of materials. By plating tin on top of a gold base and then reflowing the tin during a bonding process, a gold-tin joint is achieved between a die and a leadframe. This provides for the manufacture of gold tin alloy bumps which simplify the leadframe-to-chip bonding process as compared with tin or gold plated copper leads and gold bumps, which often result in a cracked die, or which display the tin whiskering described above.

The use of a bump comprising a tin cap upper portion 94 on a solid base lower portion 92, provides standoff height independent of any requirement for organic material attached to either the lead 84 or the die 90. Accordingly, a bump is provided for use in interconnecting electronic components which meets the organic matter prohibition of U.S. Department of Defense Military Standard 38510, and similarly restricted military standards. This results in substantially improved reliability for electronic components. Moreover, such construction facilitates the type of mass bonding known as "gang bonding" for high-density electronic devices by easing the restrictions for planarity with respect to bond height. In ther words, the individual bond heights of a plurality of bumps 98 need not be precisely the same due to the phenomenon of the tin material comprising the bump upper portion 94

providing relief for proper penetration of lead 84. This structure also facilitates repair or rework of bumps to provide overall manufacturing cost savings.

Prior art bumps comprising only gold, such as bumps 99, 100 in Figures 8 and 10, must have a height uniformity of within ± 1 micrometer. However, a preferred tin cap on solid base bump, such as bumps 101, 102 in Figures 9 and 11, allow about ± 5 micrometers of bump height non-uniformity. Thus, preferred tin cap on solid base, such as a gold or nickel base, bumps 98, 101, and 102 provide non-organic non-collapsible height standoff means while also permitting sufficient travel or penetration of conductive leads into the tin caps to achieve higher reliability during bonding over prior art bump structures.

Figures 8 and 9 show bumps manufactured using spin-on resist processes while Figures 10 and 11 show bumps manufactured using dry film resist processes. Note the novel structures shown in the tin capped bumps 101, 102 of Figures 9 and 11 respectively. These tin cap on solid base bumps overcome the bond reliability and organic matter problems of the prior art. This novel bump structure also overcomes the prior art bond site fatigue and tin whiskering problems. Even further, the high strength tin cap on solid base bump invention permits use of materials having compatible coefficients of expansion and which permit reflow and bonding at temperatures and pressures which are lower than in the prior art.

In operation, a preferred tin cap on solid base bump 98 typically comprises approximately 5 microns of tin positioned on top surface 97 of bump lower portion 92, shown generally in Figure 7, in which the bump lower portion 92 material typically comprises approximately 30 microns of solid base material, such as gold or the like. Preferably, the bonding process uses a furnace bond process to further minimize the shock of bonding leads 84 onto die 90. Thus, a method of providing a low temperature and high reliability bond between electronic components is provided. This method includes the steps of providing first and second electronic components; providing a bump for placement onto the first electronic component, the bump having a lower portion 92 comprising an effective amount of solid or non-collapsible conductive metal (e.g. gold or nickel) base material to provide non-organic standoff height during the bonding process; placing an effective amount of tin bonding material on top of th solid bas material; positioning the second electronic component proximate th tin, as shown in Figures 6 and 7 by force labels F and F′ respectively; and reflowing the tin to provid a bond between the first and second electronic components and to provide a bond between the solid base material and the tin bonding material. This method preferably includes a first electronic component comprising a lead, such as lead 84, of a leadframe, and a second electronic component comprising a die, such as die 90, which may be a semiconductor chip or wafer, or similar bump-carrying device. A preferred method of providing a low-temperature high-reliability bond between electronic components preferably comprises the step of reflowing the tin within a furnace heater.

Another method is provided according to the present tin cap on solid base bump invention. This method includes providing furnace bonding of a semiconductor chip to the conductive elements of a leadframe. This method comprises the steps of positioning a semiconductor chip comprising a plurality of bonding locations in a holding member with a chip support surface. Then, preformed bonding material is provided at the bonding locations, the preformed bonding material comprising a non-collapsible conductive metal lower portion for providing non-organic standoff height during the bonding process and a reflowable tin cap upper portion for connecting conductive elements of a leadframe with the chip bonding locations. The conductive elements of a leadframe are then aligned with corresponding bonding locations on the semiconductor chip, and the leadframe conductivo elements are moved toward the chip bonding locations so that the bonding material is arranged between the conductive elements and the chip bonding locations. A furnace bond heating process is then used for heating the bonding material to a point of reflow so that all of the conductive elements are bonded to the bonding material tin cap upper portions and the tin cap upper portions are alloyed to the non-collapsible lower portions. A further step comprises cooling the bonding material and the leadframe conductive elements.

Yet another problem within the field of electronic component packaging involves the manner of connecting leadframe conductive elements to variously spaced next levels of packaging. It is quite common for manufacturers of conductive leadframes, such as tab leadframes, to design different leadframes to match differently pitched printed circuit board footprints. However, prior art leadframes do not have structure enabling the leadframes to be used with only slight modification with differently pitched next level of packaging bond site patterns. Therefore, what has been needed has been an efficient and variable pitch tab leadframe assembly as partially shown in th fragmentary view of Figure 12.

Referring to Figure 12, a fragmentary view of a variable pitched tab leadframe assembly 103 is illustrated in which a plurality of substantially id ntical leadframe assembly segments 104 are shown

each comprising patterned conductive elements 107 for transmitting input and output signals to bonding locations 110 on an electronic device. Variable pitch tab leadframe assembly 103 also comprises means for providing a variable pitch to conductive elements 107 to accommodate a plurality of standard pitch bond site printed circuit board footprints, such as footprints designated by JEDEC standards. Figure 12 shows a fragment of a typical tab leadframe assembly according to the variable pitch leadframe assembly invention and may be appreciated more fully in the context of Figure 13 which illustrates, in dotted lines, the relative relation of the fragment of Figure 12 when combined with other fragments to form a complete representative outline of a typical variable pitch tab leadframe assembly 103 positioned preferably as one of a plurality of such leadframe assemblies on a sprocketed tape 112. In Figures 12 and 13, a central region labelled 116 represents the area in which a die, a semiconductor chip, or the like, is placed for interconnection with variable pitch tab leadframe assembly 103.

Preferred variable pitch tab leadframe assembly segment 104 comprises means for providing a variable pitch to conductive elements 107, conductive elements 107 each comprising a first end portion 120 arranged for connection with a semiconductor chip package located in area 116. Each conductive element also comprises a second end portion 123, the location of which is selected by the manufacturer, which is arranged for connection with a next level of packaging. Preferably, first end portions 120 of adjacent conductive elements have a first pitch spacing, and second end portions 123 of said adjacent conductive elements have a second pitch spacing which is different than the first pitch spacing. In Figure 12, this relationship is represented by adjacent conductive elements first and second end portions labelled 120a, 120b, and 123a, 123b respectively. Variable pitch tab leadframe assembly segments 104 may comprise a plurality of parallel sections each having a pitch spacing corresponding to, for example, a JEDEC standard pitch spacing commonly used within the field of component packaging. For example, the pitch spacing between lead second end portions may be 50 mils (1.25mm), 40 mils (1.0mm), 25 mils (.625mm), 20 mils (0.5mm), or even less. However, as the number of leads increases and greater density of packaging is pursued, the pitch of packaging continues to decr ase. Yet each time a different pitch is used on a package, it may require a package leadframe-to-board spacing specifically for that pitch.

Thus, this variabl pitch tab leadframe invention provides leadframe assembly segments 104 which comprise conductive elements 107 for connection with a package such that the package may be connected to variously pitched next levels of packaging, and vice versa. This may be accomplished by taking a tightly pitched package and attaching a leadframe to it that has and relies on the tab design to change the leadframe-to-board pitch. Tab leadframe assembly segment 104 preferably comprises interconnect sites which are fanned out along each conductive element to various desired pitches. This permits the chip manufacturer to provide a packaged device to a variety of users depending upon the user's sophistication in bonding devices to next levels of packaging using tight pitches. In other words, one size of variable pitch tab leadframe assemblies 103 may be used on many differently pitched printed circuit boards and package arrangements by cutting conductive elements 107 for desired pitch lengths at second ends 123 from a plurality of preexisting second end pitch patterns on conductive elements 107. This results in substantial savings in that manufacturers do not have to tool new leadframes and packages for each different board or user requirement. It is to be understood that pitch spacing greater than or less than those exemplary pitch spacings indicated above are envisioned within the scope of this invention, as is the number of parallel sections on conductive elements 107 for achieving numerous different pitches.

Figure 12, therefore, illustrates a variable pitch tab leadframe assembly 103 for providing connection between a semiconductor chip package, which would be located in area 116, and a next level of packaging, which would be located in an area generally designated 126 corresponding to a printed circuit board or the like. Variable pitch tab leadframe assembly 103 also preferably comprises leadframe assembly segments 104 comprising a plurality of patterned conductive elements 107 for transmitting input and output signals to bonding locations on an electronic device. Variable pitch tab leadframe assembly 103 also preferably comprises means for providing a variable pitch pattern to conductive elements 107 each comprising a first section 130 and a second section 132 in which adjacent conductive elements are arranged in parallel, and a third section 133 in which adjacent conductive elements 107 are in non-parallel, the first and second sections being connected by the third section. Also, each conductive element 107 preferably comprises a first end portion 120 for connection with a semiconductor chip package and a second end portion 123 for connection with a next level of packaging. It is to be understood that second end portions 123 may be located at various lengths or pitches, as shown in Figures 12-16. First end portions 120 of adjacent conductive elements 107 preferably have a first pitch spacing and sec-

ond end portions 123 of said adjacent conductive elements 107 have a second pitch spacing which is different than the first pitch spacing. Thus, the pitch spacing on preferred variable pitch tab leadframe assembly 103 between adjacent conductive elements 107 differs between the first and second sections.

Although various pitch spacings may be utilized in a variable pitch tab leadframe assembly 103 of the present invention, first end portions 120 of adjacent conductive elements 107 are spaced at any practicable pitch. Similarly, the corresponding second end portions of adjacent conductive elements 107 may be spaced at a pitch of generally between about 5 mils(0.125mm) and 50 mils (1.25mm). It is appreciated that the next level of packaging user will determine the appropriate pitch for leadframe-to-board attach. For example, as illustrated in Figures 14-16, adjacent conductive element second end portions 123 comprise different pitches depending on where the conductive elements 107 are severed, as determined by the pitch of the bond sites at the next level of packaging. In Figure 14, second end portions 123 are shown positioned at corresponding bond pads 130 having a pitch P1. In contrast, Figure 15 illustrates a next level of packaging requirement with bond pads 140 having a pitch P2 that is different from pitch P1. Similarly, Figure 16 illustrates another packaging requirement for which a pitch P3 exists between bond pads 150. No prior art tab leadframe assembly is known or available with structure to accommodate the multiple next level of packaging pitch requirements as depicted in Figures 14-16, or more. However, variable pitch tab leadframe assembly 103 may be used for various pitch requirements with the great advantages of simplicity, material efficiency, and savings of electronic packaging time, and is thus preferred.

A method of providing a tab leadframe assembly is also provided which permits electrical connection between a semiconductor chip package and a next level of packaging comprising various steps. These steps preferably comprise providing a leadframe as shown substantially as in Figure 12 comprising a plurality of patterned conductive elements; arranging the pattern of the leadframe conductive elements to provide a first section 130, a second section 132, and a third section 134 in which adjacent conductive elements are arranged in parallel, and a fourth section 133 and a fifth section 135 in which adjacent conductive elements are arranged in non-parallel fanned relation and which provide interconnection between the first, second, and third sections. Further, the step of arranging the pattern of the leadframe conductive elements may comprise providing a plurality of first, second, and third sections so that the pitch spacing of adjacent conductive elements differs between the first, second, and third sections. Further sections may be included following the above method of manufacture.

It is to be understood that while certain embodiments of the present invention have been illustrated and described, the invention is not to be limited to the specific forms, sizes, or arrangements of parts described and shown above, since others skilled in the art may devise other embodiments still within the limits of the claims.

Claims

1. A method of providing a tab leadframe assembly which permits electrical connection to one of a plurality of differently pitched next level of packaging bond site footprints the method characterised by:

a) providing a variable pitch tab leadframe assembly (103) comprising a plurality of patterned conductive elements (107);

b) arranging the pattern of the leadframe conductive elements to provide a first section (130), a second section (132), and a third section (134); each section comprising adjacent conductive elements (107) arranged in parallel and with each section comprising pitch spacing (P1, P2, P3) that is different from the other sections; and

c) positioning a leadframe conductive element fourth section (133) in connection with the first (130) and second (132) sections, and a fifth section (135) in connection with the second section (132) and the third section (134) so that adjacent conductive elements (107) in each of the fourth (133) and fifth (135) sections are positioned in non-parallel relation.

2. A variable pitch tab leadframe assembly (103) characterised by:

a) tape carrier material; and

b) a plurality of patterned conductive elements (107) adjacently arranged on the tape carrier material in a plurality of sections, comprising:

i) a first section (130), a second section (132), and a third section (134), each section comprising adjacent conductive elements (107) arranged in parallel and arranged with a pitch spacing (P1, P2, P3) that is different than the pitch spacing of the elements (107) in the other two sections;

ii) a fourth section (133) providing connection between the first section (130) and the second section (132), and a fifth section (135) providing connection between the second section (132) and the third section (134) so that adjacent conductiv elements (107) in each of the fourth and fifth sections are positioned in non-parallel relation;

c) wherein the variable pitch tab leadframe assembly (103) permits electrical connection between a semiconductor chip package (126) and one of a plurality of differently pitched next level of packaging bond sites.

EP 0 393 997 A2

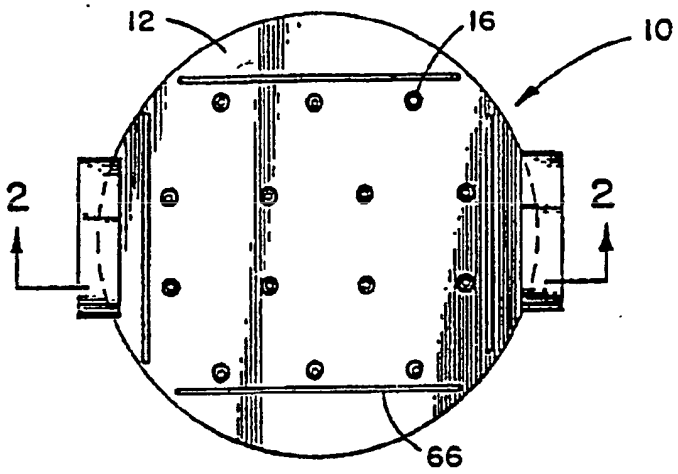


FIG. 1

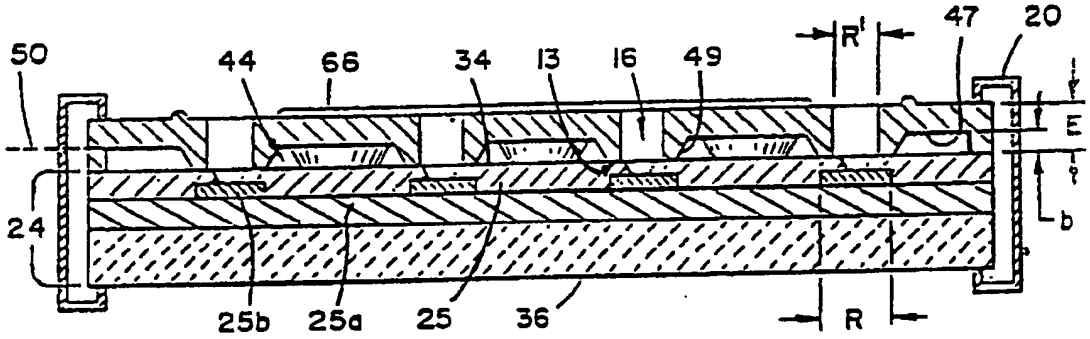
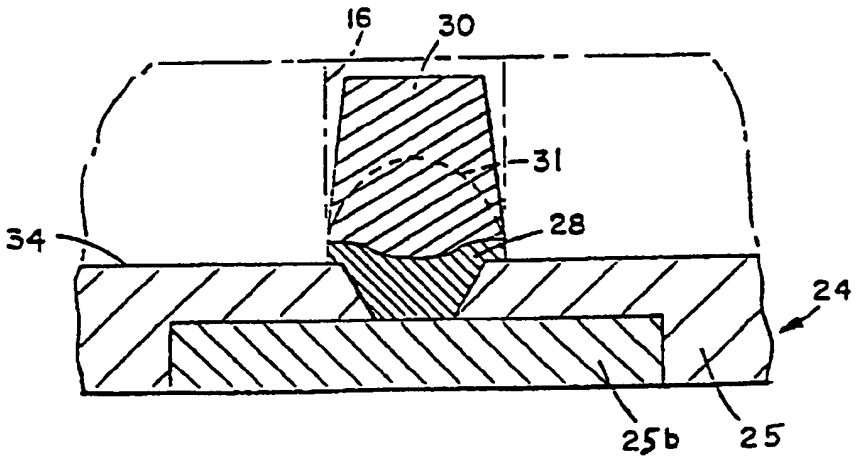


FIG. 2



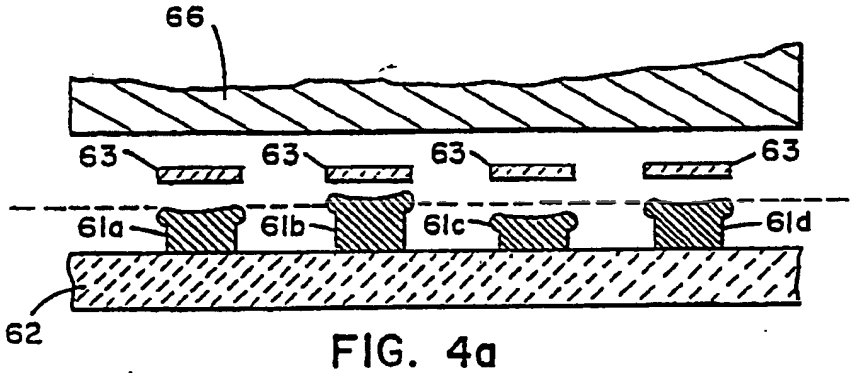


FIG. 4a

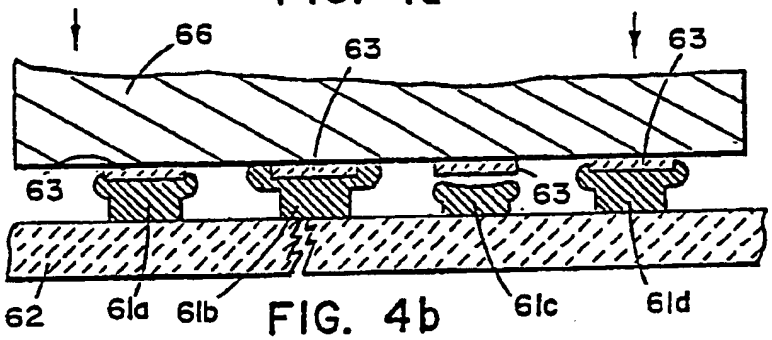


FIG. 4b

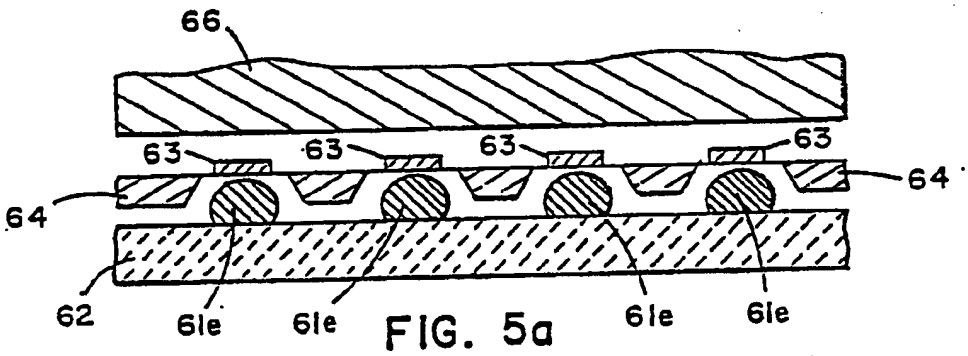


FIG. 5a

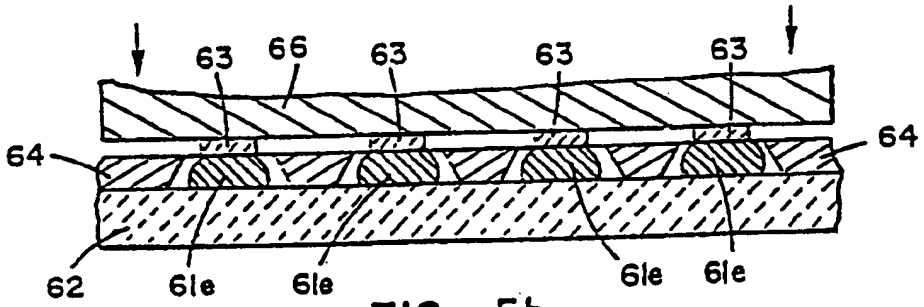


FIG. 5b

EP 0 393 997 A2

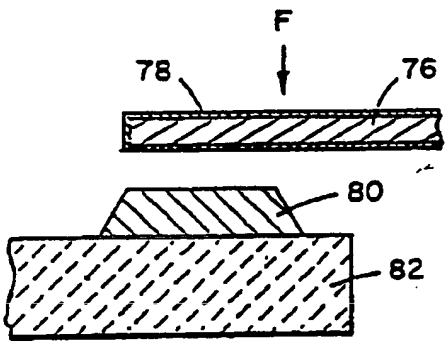


FIG. 6 (PRIOR ART)

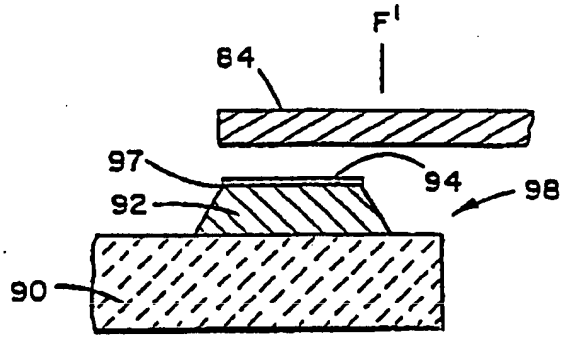


FIG. 7

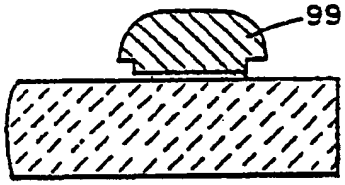


FIG. 8 (PRIOR ART)

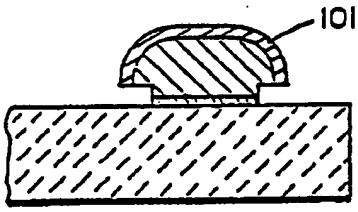


FIG. 9

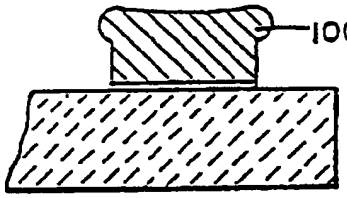


FIG. 10 (PRIOR ART)

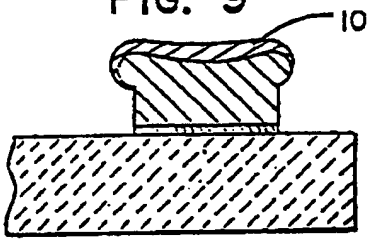


FIG. 11

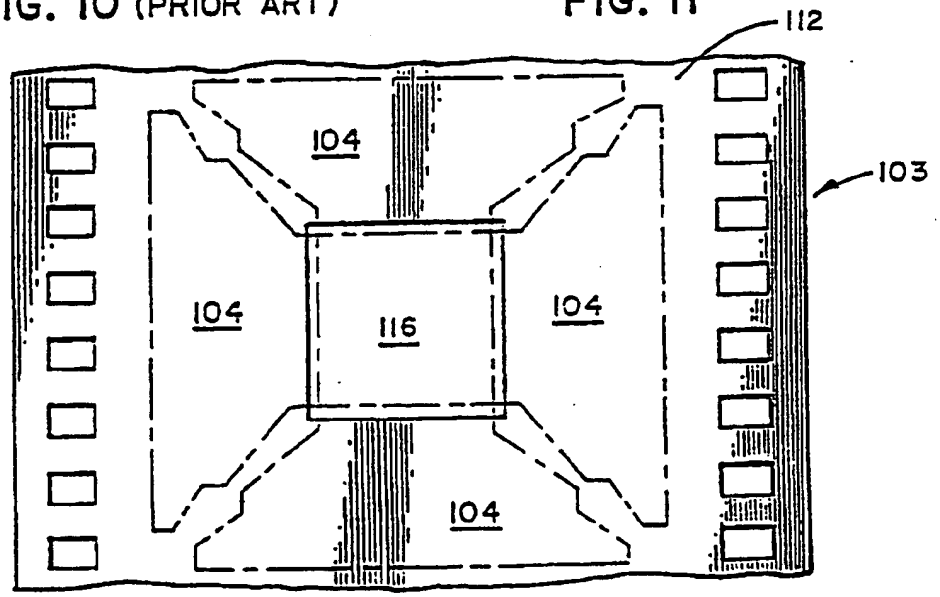


FIG. 13

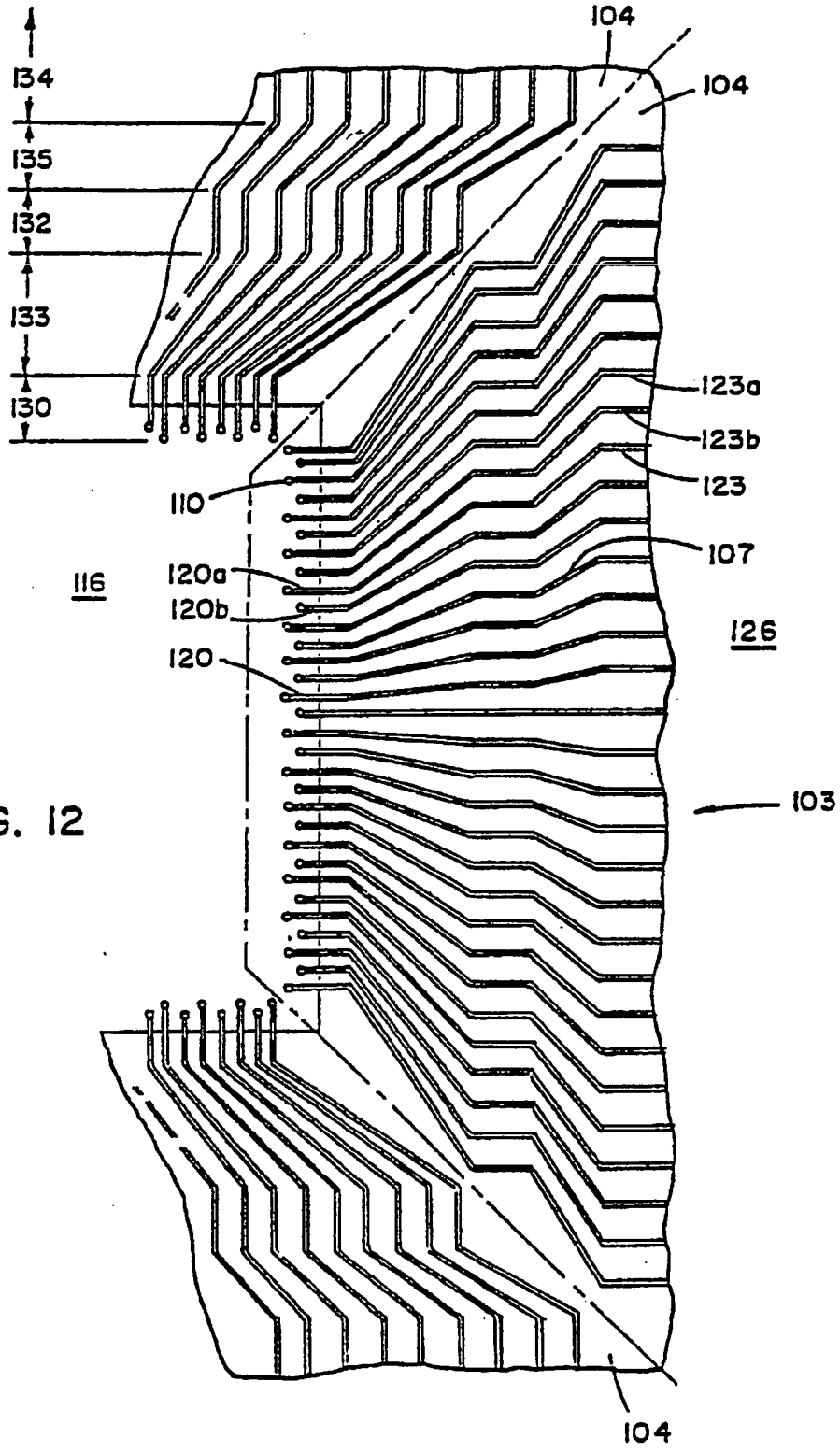

104
104
134
135
132
133
130
123a
123b
123
110
107
116
120a
120b
126
120
103
104

FIG. 12

FIG. 14

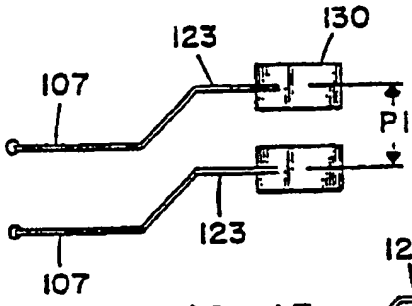


FIG. 15

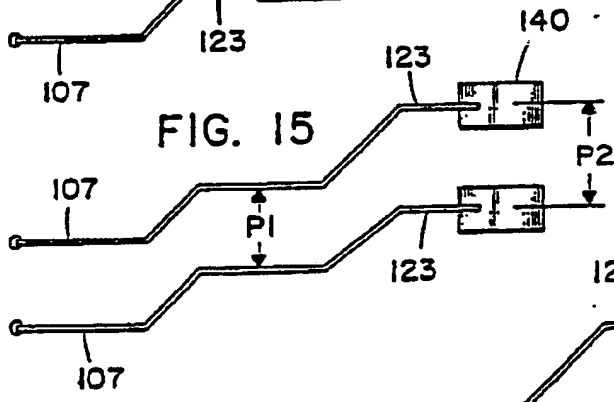


FIG. 16